CCD5045
Time Delay Integration Line Scan Sensor

FEATURES

- 4096 Active Pixels per Line
- 96 TDI Lines
- 13µm x 13µm Pixels
- 4 High Speed Output Ports
- TDI Stages Selectable Between 96, 64, 32, 16, or 4
- 132 MHz Data Rate with 4 Outputs Operating at 33 MHz
- 30.6 kHz Maximum Line Rate
- 2000X Antiblooming Protection
- High Sensitivity

GENERAL DESCRIPTION

The CCD5045 is a Time Delay Integration (TDI) sensor designed for a wide range of imaging applications requiring high speed operation combined with high sensitivity. The sensor is capable of producing a total data rate of 132 MHz (line rate > 30 kHz). The CCD has a total imaging area of 4096 contiguous elements by 96 TDI rows. The pixel dimensions are 13µm by 13µm. The CCD overall dimensions are 54.5 mm x 3.3 mm. The sensor is mounted in a custom 48-pin, 600 mil dual-in-line ceramic package.

The CCD5045 imaging area is controlled by 3-phase timing, and exposure control is performed by selecting the number of active TDI stages. Independent TDI control gates allow the following number of TDI stages to be selected: 96, 64, 32, 16, or 4. The CCD5045 features lateral antiblooming structures capable of 2000X over-saturation protection.

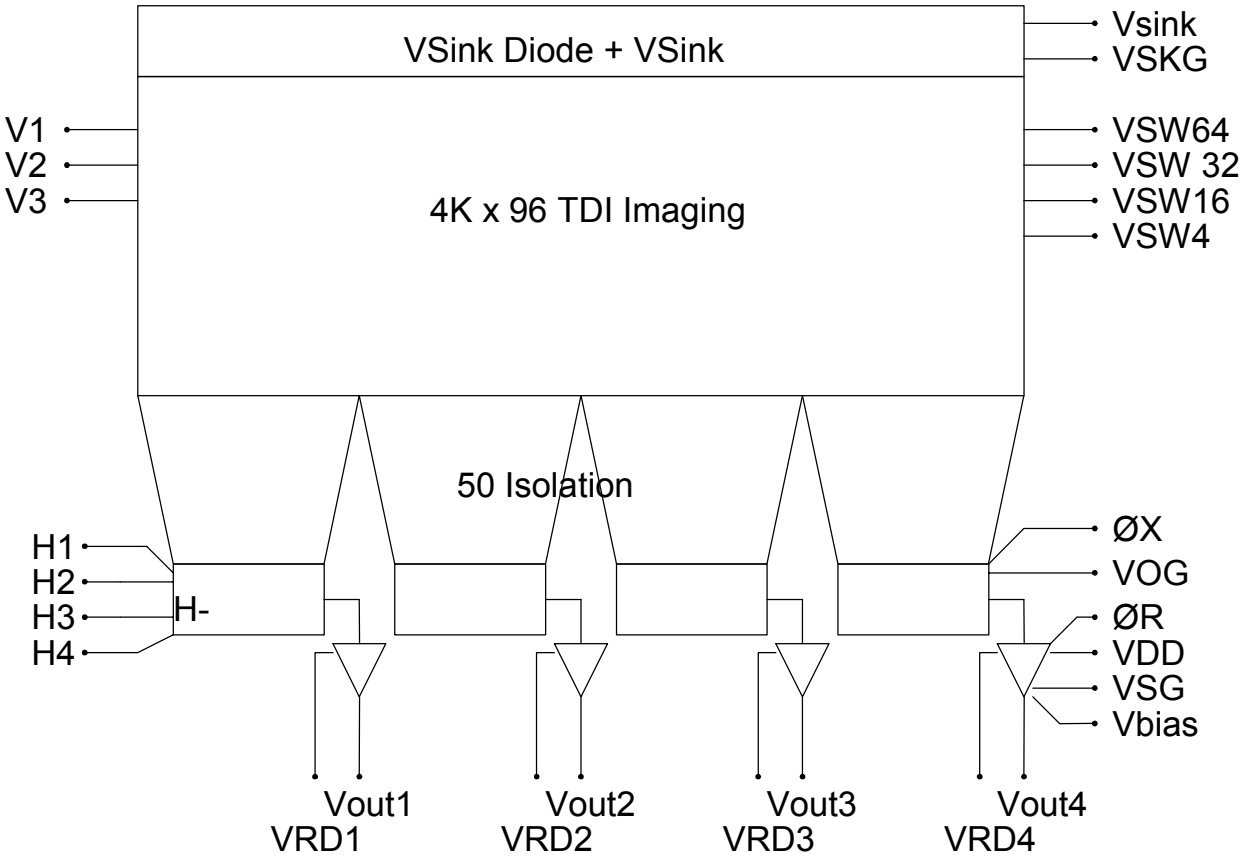
The vertical (parallel) imaging register is separated from the horizontal (serial) registers by 50 isolation rows. The isolation rows are also controlled by 3-phase timing. The isolation rows are covered with a light shield and are used to transfer the charge from the imaging area to four horizontal registers. The horizontal registers are controlled by 4-phase timing. The design of the horizontal registers has been optimized for high charge transfer efficiency at low signal levels.

Each horizontal register is connected to a high-speed output amplifier. The output amplifier is a three-stage source follower designed for high conversion gain and extended bandwidth.

DEVICE ARCHITECTURE

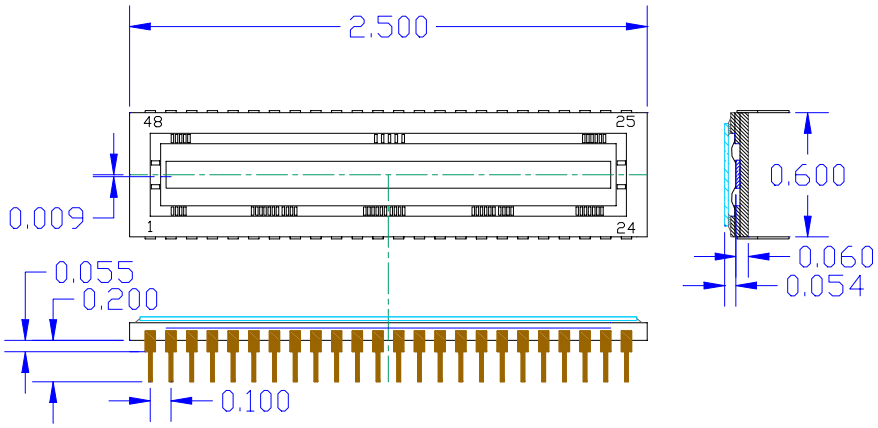
The CCD5045 operates in buried channel mode for optimal performance. The imaging area consists of 4096 contiguous pixels by 96 rows. Photogenerated charge is integrated in this region, then following the integration time, the charge is transferred line by line to the adjacent isolation rows for readout. The number of active TDI rows is simply controlled by biasing the appropriate control gates, VSWxx, low. Normal vertical timing is employed across the array irrespective of the selected number of active TDI stages. The last gate in the vertical register is also called the vertical transfer gate, ΦX. The charge is transferred from the vertical register to the horizontal registers when ΦX is clocked low. The horizontal registers require 4-phase timing. Charge is transferred, pixel by pixel, to the floating diffusion sense node where it produces a voltage change corresponding to the signal level. After the signal is sampled, the reset gate is clocked high to clear the signal, and restore the potential of the sense node to the VRD reset drain voltage. There are three prescan elements in each video line.

CCD5045 Block Diagram



PACKAGE INFORMATION

The CCD5045 is mounted in a ceramic dual-in-line package with 48 pins. The spacing between each pin is 0.100” and the distance between the two rows of pins is 0.600”. The overall dimensions of the package are 2.50” x 0.610” x 0.115”. The package window is covered with an antireflection (AR) coated cover glass.



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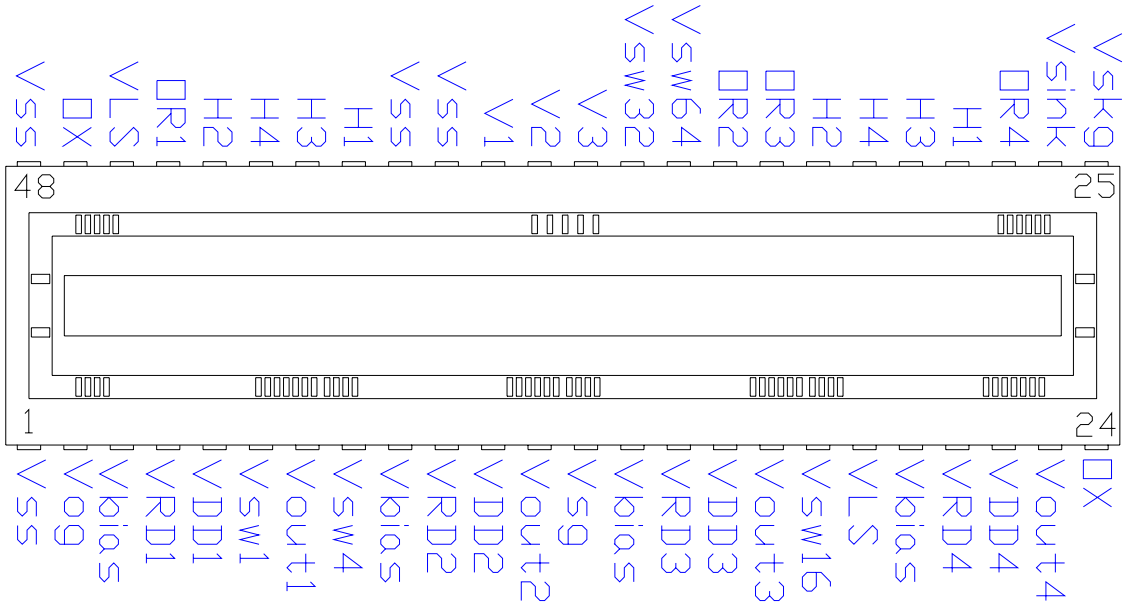
Package Pin Assignment

Pin Name and Description



Pin	Pin Name	Description	Pin	Pin Name	Description
1	VSS	Substrate	25	VSKG	Overflow gate bias
2	VOG	Output gate	26	Vsink	Overflow drain bias
3	Vbias	Current source bias	27	ΦR4	Reset gate
4	VRD1	Output 1 reset drain	28	H1	Horizontal CCD clock phase 1
5	VDD1	Amplifier supply	29	H3	Horizontal CCD clock phase 3
6	VSW1	TDI 1 select gate	30	H4	Horizontal CCD clock phase 4
7	Vout1	Video output 1	31	H2	Horizontal CCD clock phase 2
8	VSW4	TDI 4 select gate	32	ΦR3	Reset gate
9	Vbias	Current source bias	33	ΦR2	Reset gate
10	VRD2	Output 2 reset drain	34	VSW64	TDI 64 select gate
11	VDD2	Amplifier supply	35	VSW32	TDI 32 select gate
12	Vout2	Video output 2	36	V3	Vertical CCD clock phase 3
13	VSG	Amplifier supply return	37	V2	Vertical CCD clock phase 2
14	Vbias	Current source bias	38	V1	Vertical CCD clock phase 1
15	VRD3`	Output 3 reset drain	39	VSS	Substrate
16	VDD3	Amplifier supply	40	VSS	Substrate
17	Vout3	Video output 3	41	H1	Horizontal CCD clock phase 1
18	VSW16	TDI 16 select gate	42	H3	Horizontal CCD clock phase 3
19	VLS	Light shield ground	43	H4	Horizontal CCD clock phase 4
20	Vbias	Current source bias	44	H2	Horizontal CCD clock phase 2
21	VRD4	Output 4 reset drain	45	ΦR1	Reset gate
22	VDD4	Amplifier supply	46	VLS	Light shield ground
23	Vout4	Video output 4	47	ΦX	Vertical transfer gate
24	ΦX	Vertical transfer gate	48	VSS	Substrate

Absolute Maximum Ratings

Description	Min	Max	Units	Remarks
Diode voltages	0	28	V	Pins VRD, VDD, VSS, Vout, Vsink
CCD gate voltages	-16	16	V	Pins V1, V2, V3, H1, H2, H3, H4
Single gate voltages	-5	16	V	Pins ΦR, ΦX, VOG, VSDKG
Gate-to-gate voltages		16	V	
Storage temperature	-50	+65	ºC	
Humidity	30	80	%RH	

DC Operating Characteristics

Pin Name	Description	Min	Typical	Max	Units & Tolerance
VDD	Amplifier supply	+13.5	+14	+14.5	V ± 5%
VSG	Amplifier supply return	+0.5	+0.7	+0.9	V ± 5%
Vbias	Current source bias	+1.5	+2	+2.5	V ± 5%
VRD	Output reset drain	+10	+10.5	+11	V ± 5%
VOG	Output gate	+0.5	+1	+1.5	V ± 5%
VSS	Substrate	0	0	0	V ± 5%
VLS	Light shield voltage	0	0	0	V ± 10%
Vsink	Overflow drain bias	+13.5	+14	+14.5	V ± 10%
VSKG	Overflow gate bias	-2.5	-2	-1.5	V ± 10%
VSWxx	TDI select gate (xx=4, 16, 32, 64)	-6.5	-6	-5.5	V ± 5%

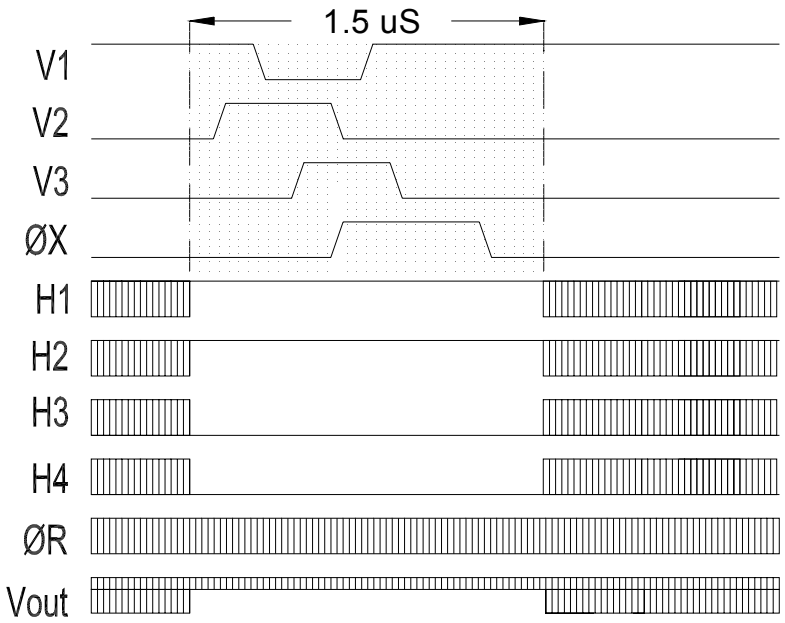
AC Operating Characteristics

Pin Name	Description	Level	Min	Typical	Max	Units & Tolerance
V1, V2, V3	Vertical CCD gate	Low	-1	0	0	V ± 10%
		High	+9.5	+10	+10.5	V ± 10%
H1, H2, H3, H4	Horizontal CCD gate	Low	-1	0	0	V ± 10%
		High	+5.0	+5.2	+6.5	V ± 10%
ΦR1, 2, 3, 4	Reset gate	Low	+0.5	+5	+5.5	V ± 10%
		High	+8.5	+9	+10	V ± 10%
ΦX	Vertical transfer gate	Low	-1	0	0	V ± 10%
		High	+9.5	+10	+10.5	V ± 10%
VSWxx	TDI select gate (xx= 4, 16, 32, 64)	Low	-1	0	0	V ± 10%
		High	+9.5	+10	+10.5	V ± 10%
IDD	Amplifier current per output		4	5	9	mA

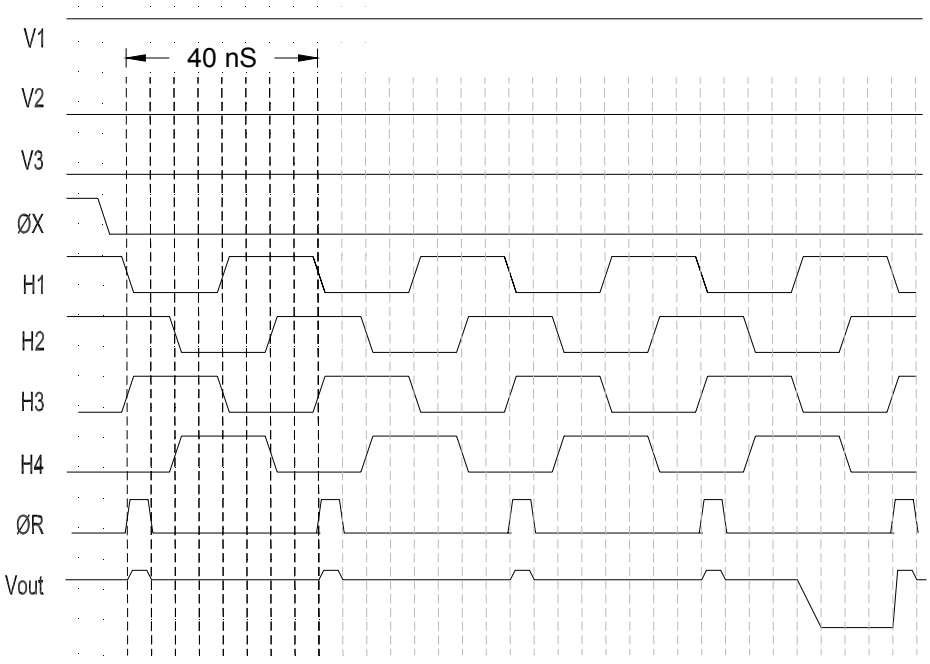
Gate Capacitance

Pin Name	Description	Effective Capacitance	Remarks
V1, V2, V3	Vertical CCD gate	7600pF	Per phase
H1, H2, H3, H4	Horizontal CCD gate	190pF	Per phase
ΦR1, 2, 3, 4	Reset gate	6pF	Per gate
ΦX	Vertical transfer gate	120pF	Per gate
VSWxx	TDI select gate (xx = 1, 4, 16, 32, 64)	240pF	Per gate

CCD Clock Timing



CCD 545 VERTICAL TIMING



CCD 545 HORIZONTAL CLOCK TIMING

Performance Specifications

Description	Symbol	Min	Typical	Max	Units	Remarks
Vertical saturation charge	Qsat	150	200	-	Ke-	
QE at 650 nm	QE	20	22	-	%	
Readout noise	Noise	-	70	100	e-	
Dynamic range	DR	2700	3000	-		
Horizontal CTE	HCTE	0.9999	0.99995	-		Per transfer
Vertical CTE	VCTE	0.999	0.9995	-		Per transfer
Photoresponse non-uniformity	PRNU	-	5	10	%	TDI = 96
Dark current	Idark	-	1	-	nA/cm^2	
Dark signal charge density	Idark	-	10500	-	Elec/pixel/sec	
Dark signal non-uniformity	DSNU	-	< 5%	-	Qsat	
Output amplifier DC offset		-	10.3	-	Vdc	
Output amplifier sensitivity		2.5	3	3.5	µV/e-	
Antiblooming	AB	1500	2000	-		X saturation
Peak responsitivity	Resp.	-	320	-	$V/\mu j/cm^2$	At 650 nm
Test Conditions: Tests were performed at 25ºC with horizontal clock frequency of 25 MHz per output and vertical clock frequency of 23 kHz.						

CCD HANDLING

CCD sensors are very sensitive to ESD damage, therefore strict static-safe handling precautions must be carefully observed during their use. Evidence of ESD damage resulting from improper handling may invalidate the warranty.

- The work station and the operator must be fully grounded when the CCD is removed from its shorting bars or conductive foam.
- The receiving socket and associated circuitry must be adequately grounded.
- The CCD must be stored with proper shorting bars attached or mounted in conductive foam.

WARRANTY

Within twelve months of delivery to the end customer, Fairchild Imaging will repair or replace, at our option, any Fairchild Imaging product if any part is found to be defective in materials or workmanship. Contact Customer Service for assignment of warranty return number and shipping instructions to ensure prompt repair or replacement.

CERTIFICATION

Fairchild Imaging certifies that its products are fully inspected and tested at the factory prior to shipment and that they conform to the stated specifications.

This product is designed, manufactured and distributed utilizing the ISO 9000:2000 Business Management System.

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